Low Supply Current, 50mW Stereo Cap-Free Headphone Driver

Features

- **Operating Voltage: 2.3V~5.5V**
- **Supply Current**
  - **I_{DD}=1mA at V_{DD}=3.6V**
- **Low Shutdown Current**
  - **I_{DD}=5μA at V_{DD}=3.6V**
- **Ground Reference Output**
  - **No Output Capacitor Required (for DC Blocking)**
  - **Save the PCB Space**
  - **Reduce the BOM Costs**
  - **Improve the Low Frequency Response**
- **Output Power 50mW/Ch into 16Ω at V_{DD}=3.6V**
- **High PSRR: 80dB at 217Hz**
- **Fast Start-Up Time: 4ms**
- **Integrate the De-pop Circuitry**
- **Thermal Protection**
- **Integrated LDO (Low Dropout Regulator) for Microphone Detection Circuit (1.9V)**
- **Surface-Mount Packaging**
  WLCSP1.6x1.6-12
- **Lead Free and Green Devices Available (RoHS Compliant)**

Applications

- **Handsets**
- **PDAs**
- **Portable Multimedia Devices**
- **Notebooks**

General Description

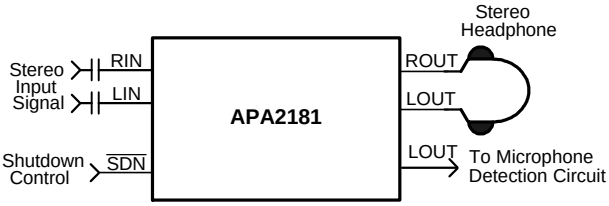
The APA2181 is a stereo, fixed gain, single supply, and cap-free headphone driver, which is available in a WLCSP1.6x1.6-12 package.

The APA2181 is ground-reference output, and no need the output capacitors for DC blocking. The advantages of eliminating the output capacitor are saving the cost, eliminating component height, and improving the low frequency response.

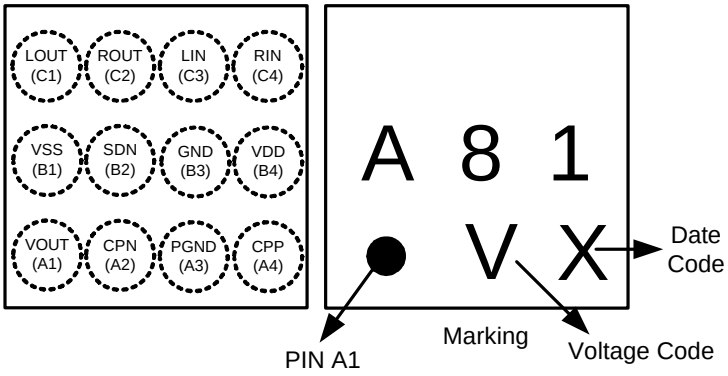
The internal fixed gain setting (-1.5V/V) can minimize the external component counts and save the PCB space. High PSRR provides increased immunity to noise and RF rectification. LDO is the best solution for microphone detection circuit requirement, and it can lower the total BOM costs.

The APA2181 is capable of driving 50mW at 3.6V into16Ω load, and provides thermal protection.

Simplified Application Circuit



Pin Configuration



WLCSP1.6x1.6-12
(Top View)

Ordering and Marking Information

APA2181 □□□□-□□□ Assembly Material Handling Code Temperature Range Package Code Voltage Code	Voltage Code D : 1.9V M : 2.8V Package Code HA : WLCSP1.6x1.6-12 Temperature Range I : - 40 to 85 °C Handling Code TR : Tape & Reel Assembly Material G : Halogen and Lead Free Device
APA2181 HA: A81 • VX	X - Date Code ; V - Voltage Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit
V_{PGND_GND}	PGND to GND Voltage	-0.3 to 0.3	V
V_{DD}	Supply Voltage (VDD to GND and PGND)	-0.3 to 5.5	
$V_{\overline{SDN}}$	Input Voltage ($\overline{SDN}$ to GND)	GND-0.3 to V_{DD}+0.3	
V_{SS}	VSS to GND and PGND Voltage	-5.5 to 0.3	
V_{OUT}	ROUT and LOUT to GND Voltage	V_{SS}-0.3 to V_{DD}+0.3	
V_{CPP}	CPP to PGND Voltage	PGND-0.3 to V_{DD}+0.3	
V_{CPN}	CPN to PGND Voltage	PV_{SS}-0.3 to PGND+0.3	
T_J	Maximum Junction Temperature	150	°C
T_{STG}	Storage Temperature Range	-65 to +150	

Absolute Maximum Ratings (Cont.) (Note 1)

Symbol	Parameter	Rating	Unit
T_{SDR}	Maximum Soldering Temperature Range, 10 Seconds	260	°C
P_D	Power Dissipation	Internally Limited	W

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ_{JA}	Thermal Resistance - Junction to Ambient (Note 2) WLCSP1.6x1.6-12	160	°C/W

Note 2: Please refer to "Thermal Pad Consideration". 2 layered 5 in2 printed circuit boards with 2oz trace and copper through several thermal vias. The thermal pad is soldered on the PCB.

Recommended Operating Conditions

Symbol	Parameter		Range	Unit
V_{DD}	Supply Voltage		2.3 ~ 5.5	V
V_{IH}	High Level Threshold Voltage	$\overline{SDN}$	1.0 ~ V_{DD}	
V_{IL}	Low Level Threshold Voltage	$\overline{SDN}$	0 ~ 0.35	
T_A	Operating Ambient Temperature Range		-40 ~ 85	°C
T_J	Operating Ambient Temperature Range		-40 ~ 125	
R_L	Headphone Resistance		16 ~ 100k	Ω

Electrical Characteristics

V_{DD}=3.6V, V_{GND}=V_{PGND}=0V, $V_{\overline{SDN}}$=V_{DD}, C_{CPF}=C_{CPO}=1μF, C_i=1μF, T_A=25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA2181			Unit
			Min.	Typ.	Max.	
I_{DD}	V_{DD} Supply Current		-	1	2	mA
I_{SD}	V_{DD} Shutdown Current	$V_{\overline{SDN}}$=0V	-	5	10	μA
I_I	Input current	$\overline{SDN}$	-	0.1	-	
CHARGE PUMP						
f_{OSC}	Switching Frequency		400	500	600	kHz
R_{eq}	Equivalent Resistance		-	15	18	Ω
DRIVERS						
A_V	Internal Voltage Gain	No Load	-1.55	-1.5	-1.45	V/V
$\triangle A_V$	Gain Matching		-	1	2	%
R_i	Input Resistance		12	14	16	kΩ
R_f	Feedback Resistance		17	21	25	
V_{SR}	Slew Rate		-	2.5	-	V/μs
V_{OS}	Output Offset Voltage	V_{DD}=2.3V to 5.5V, R_L = 16Ω	-8	-	8	mV
V_N	Output Noise		-	27	-	μVrms

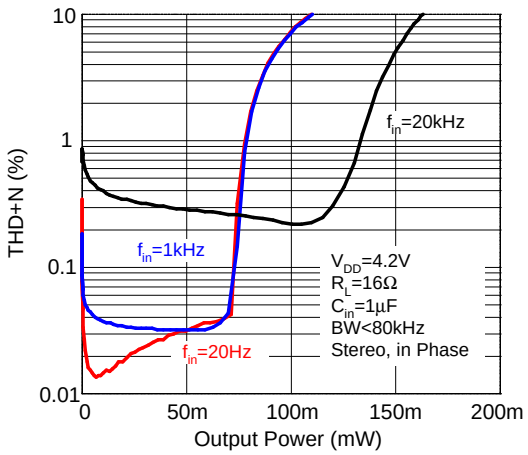
Electrical Characteristics (Cont.)

V_{DD}=3.6V, V_{GND}=V_{PGND}=0V, $V_{\overline{SDN}}$=V_{DD}, C_{CPF}=C_{CPO}=1µF, C_i=1µF, T_A=25°C (unless otherwise noted)

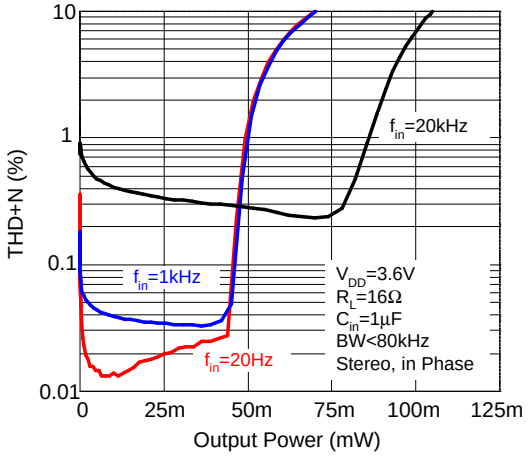
Symbol	Parameter	Test Conditions	APA2181			Unit
			Min.	Typ.	Max.	
DRIVERS (CONT.)						
PSRR	Power Supply Rejection Ratio	V_{DD}=2.3V to 5.5V, V_{rr}=200mVrms f_{in}= 217Hz f_{in}= 1kHz f_{in}= 20kHz	-	 -80 -80 -40	 -60 -60 -35	dB
C_L	Maximum Capacitive Load		-	400	-	pF
$T_{start-up}$	Start-up Time		-	4	-	ms
V_{ESD}	ESD Protection	OUTR, OUTL	-	8	-	kV
P_O	Output Power (Stereo, In Phase)	THD+N=1%, f_{in}=1kHz R_L=16Ω R_L=32Ω	 45	 50 60	 -	mW
		THD+N=10%, f_{in}=1kHz R_L=16Ω R_L=32Ω	-	 70 80	 -	
THD+N	Total Harmonic Distortion Plus Noise	P_O=20mW, R_L=32Ω f_{in}=20Hz f_{in}=1kHz f_{in}=20kHz	-	 0.03 0.03 0.20	 -	%
Crosstalk	Channel Separation	P_O=40mW, R_L=32Ω, f_{in}=20Hz f_{in}=1kHz f_{in}=20kHz	75	 85 85 70	 -	dB
S/N	Signal to Noise Ratio	V_{DD}=5V, P_O=140mW, R_L=32Ω, With A-weighting Filter	-	95	-	
LDO (LOW DROP-OUT REGULATOR)						
V_O	Output Voltage Accuracy	Over Temp & Over Load Current	-	±5	-	%
I_O	Output Current		5	-	-	mA
I_{LIM}	Current-Limit		30	40	50	
I_{SC}	Short Circuit Current-Limit		6	8	10	
PSRR	Power Supply Rejection Ratio	I_O=1mA, f_{in}=1kHz	-	40	-	dB

Typical Operating Characteristics

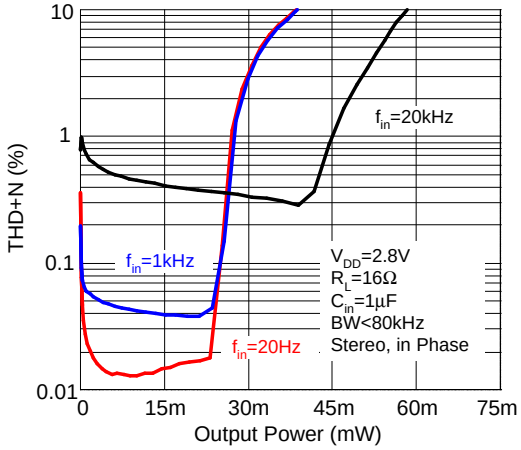
THD+N vs. Output Power



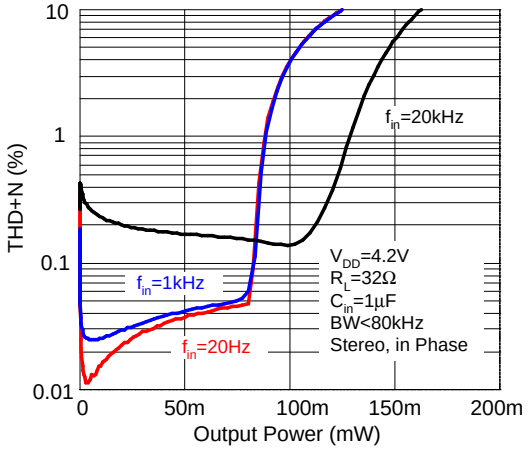
THD+N vs. Output Power



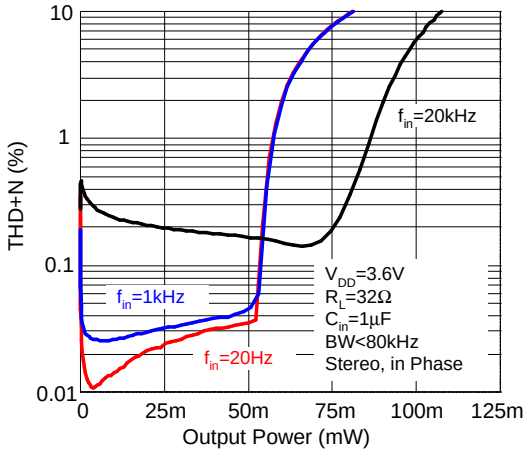
THD+N vs. Output Power



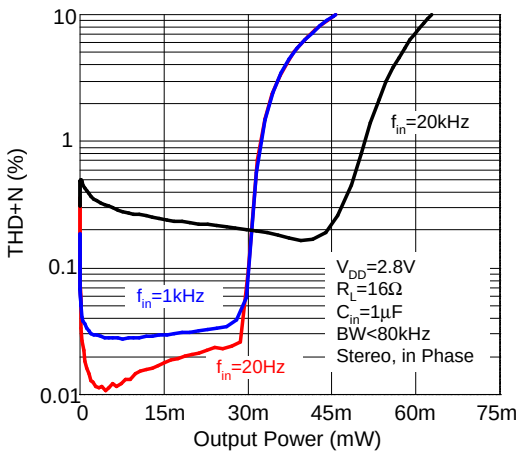
THD+N vs. Output Power



THD+N vs. Output Power

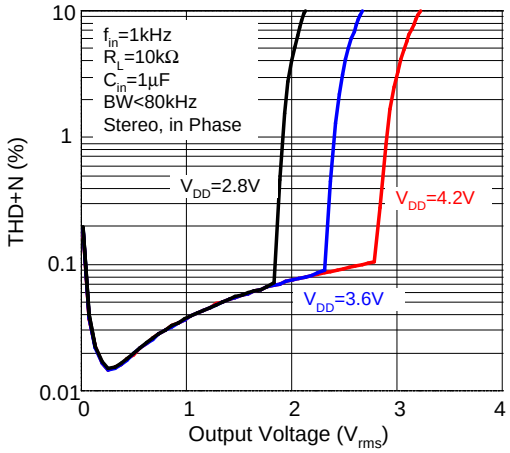


THD+N vs. Output Power

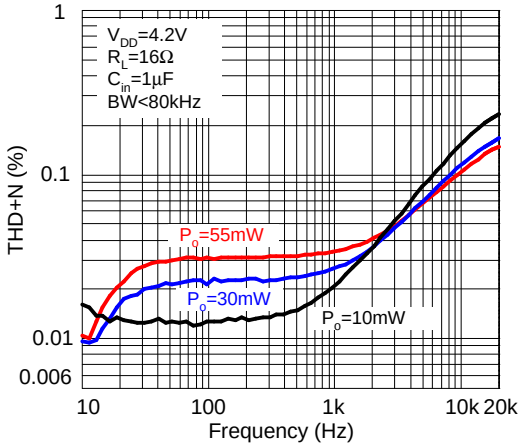


Typical Operating Characteristics (Cont.)

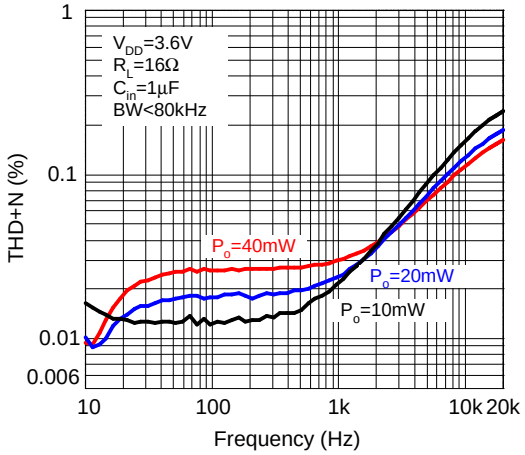
THD+N vs. Output Voltage



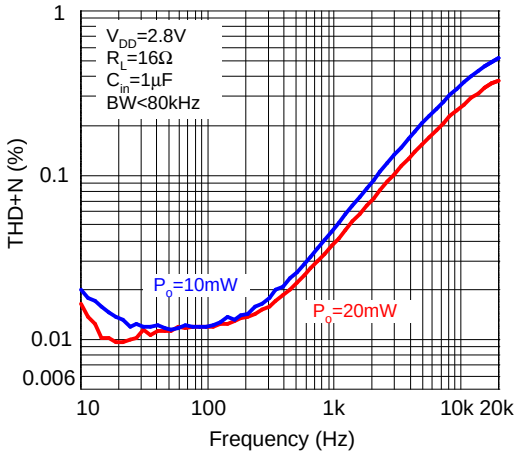
THD+N vs. Frequency



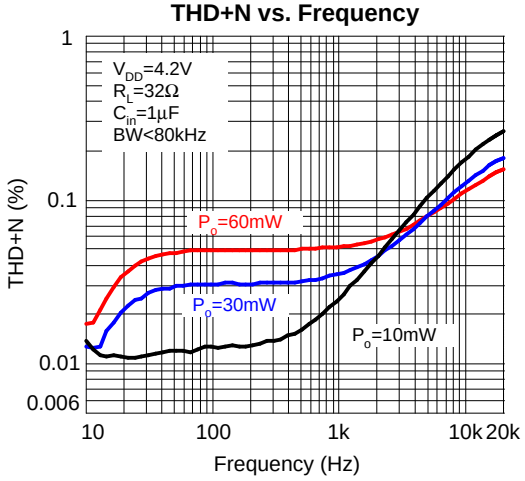
THD+N vs. Frequency



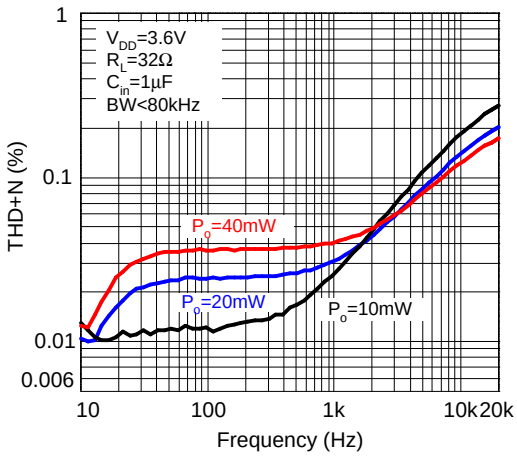
THD+N vs. Frequency



THD+N vs. Frequency

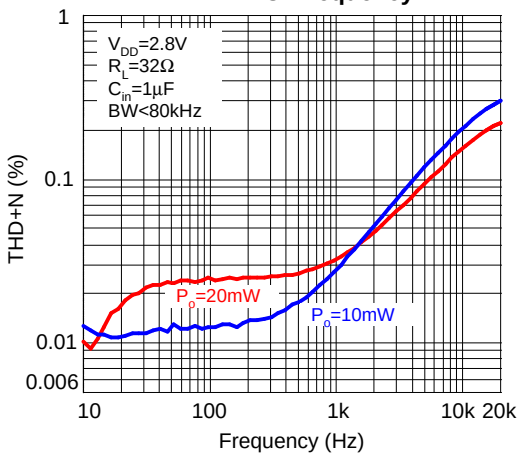


THD+N vs. Frequency

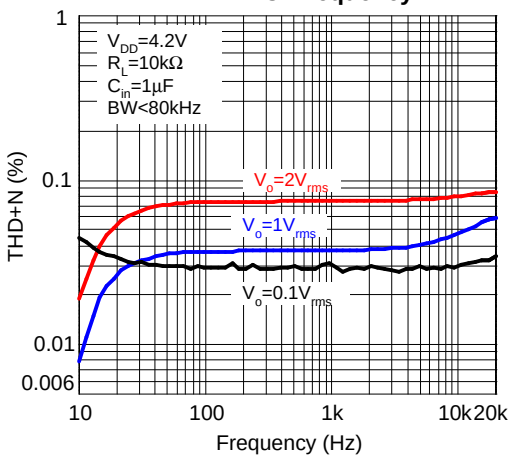


Typical Operating Characteristics (Cont.)

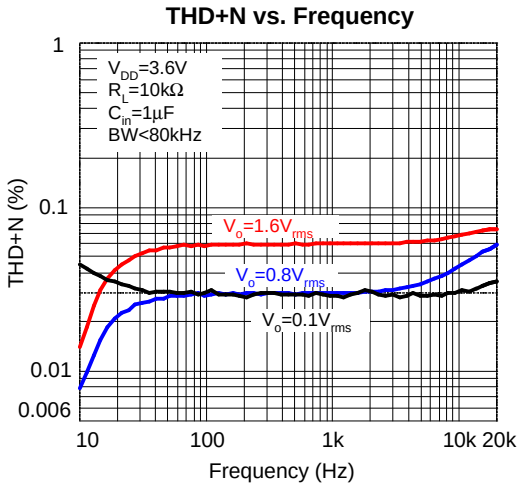
THD+N vs. Frequency



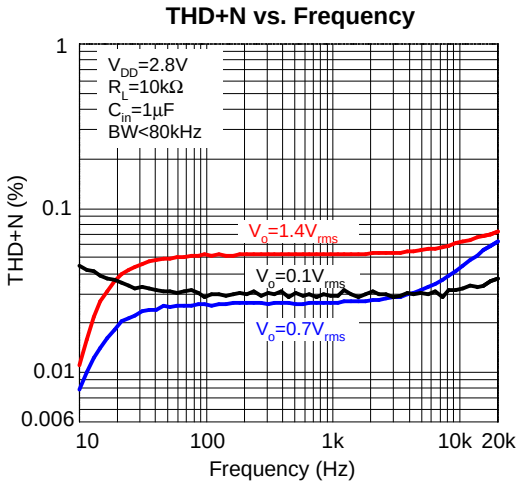
THD+N vs. Frequency



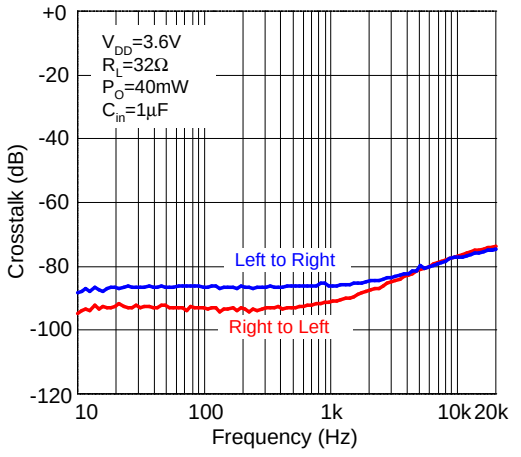
THD+N vs. Frequency



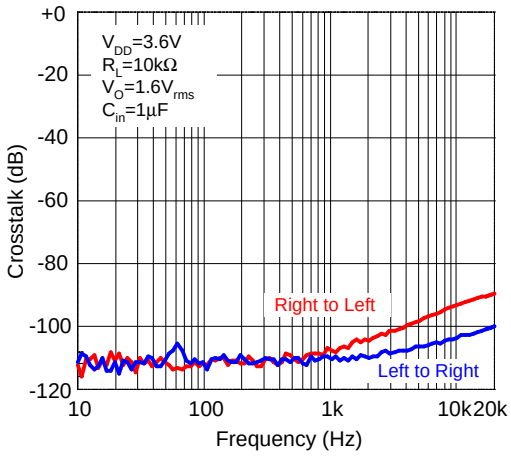
THD+N vs. Frequency



Crosstalk vs. Frequency

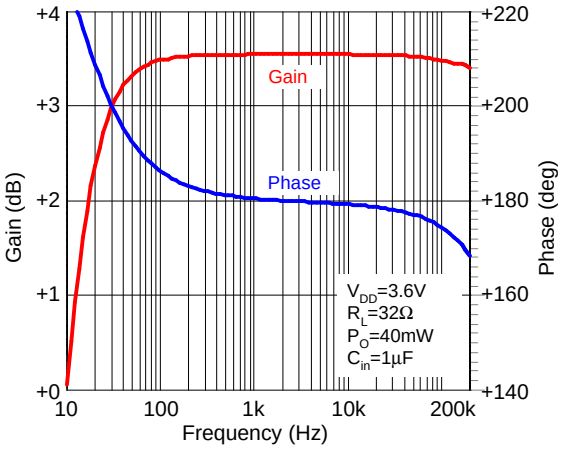


Crosstalk vs. Frequency

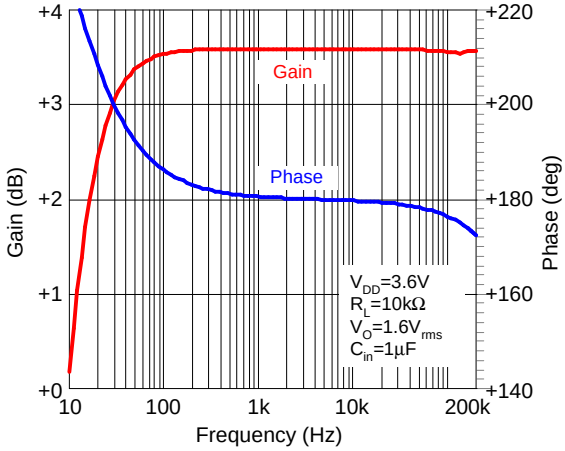


Typical Operating Characteristics (Cont.)

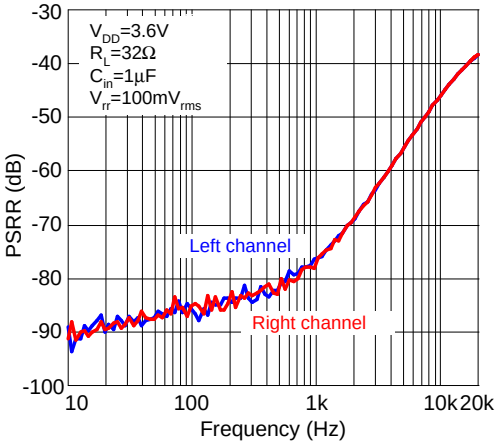
Frequency Response



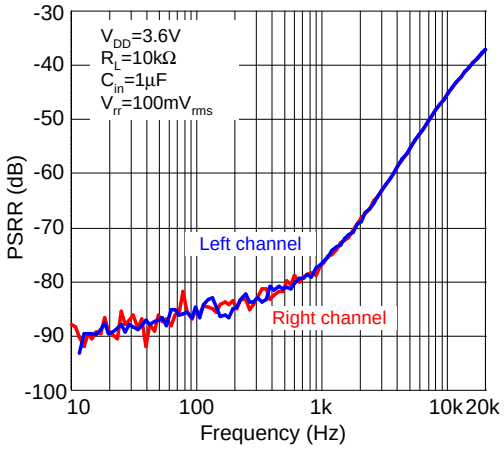
Frequency Response



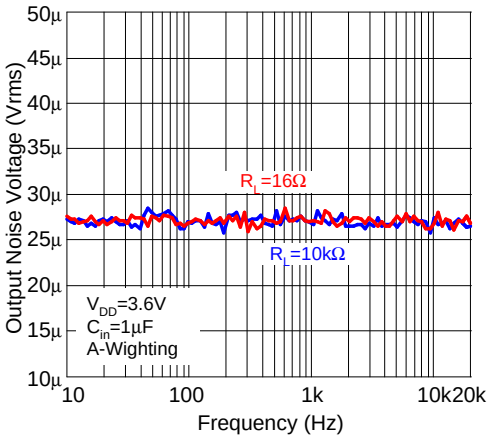
PSRR vs. Frequency



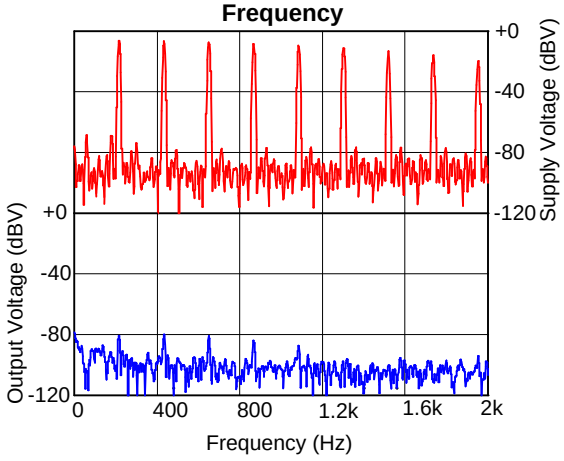
PSRR vs. Frequency



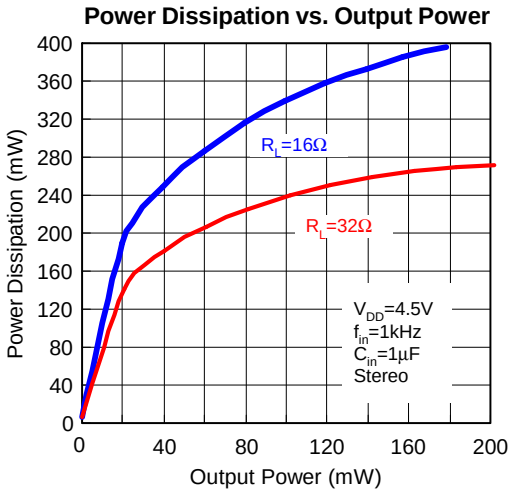
Output Noise Voltage vs. Frequency

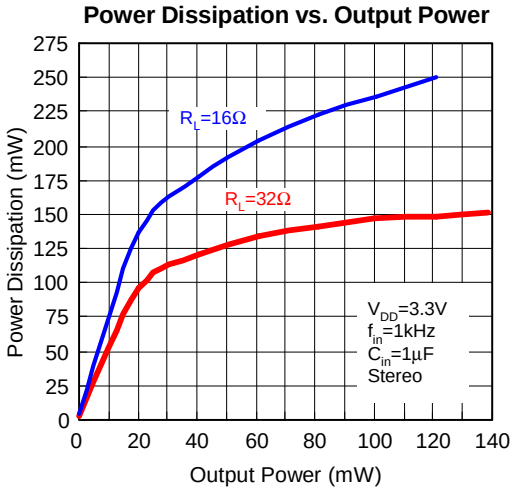


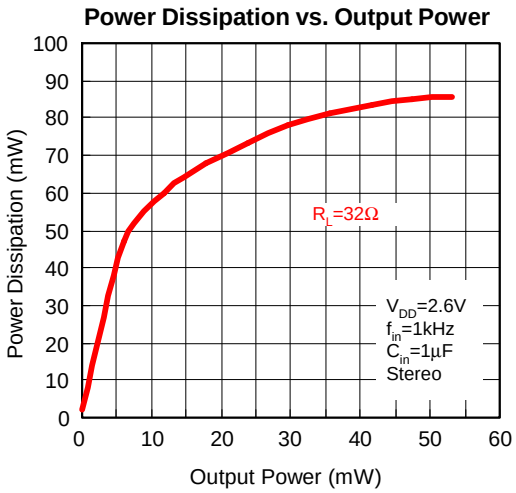
GSM Power Supply Rejection vs. Frequency



Typical Operating Characteristics (Cont.)

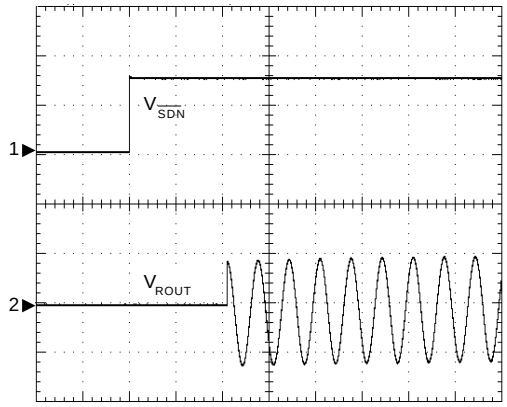






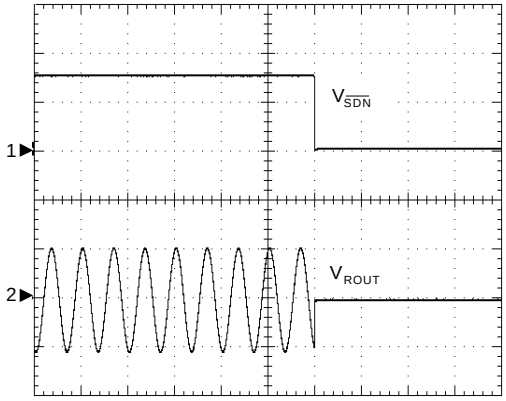
Operating Waveforms

Shutdown Release



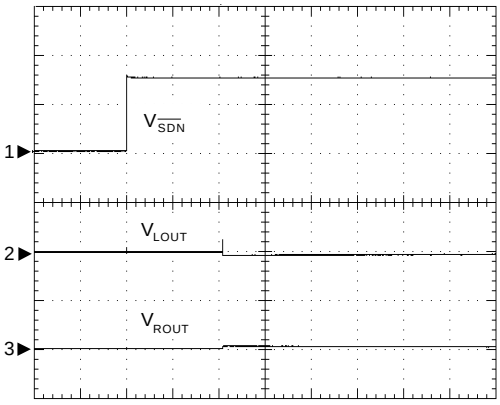
V_{DD}=3.6V, R_L=32Ω
CH1: $V_{\overline{SDN}}$, 2V/Div, DC
CH2: V_{ROUT}, 1V/Div, DC
TIME:2ms/Div

Shutdown



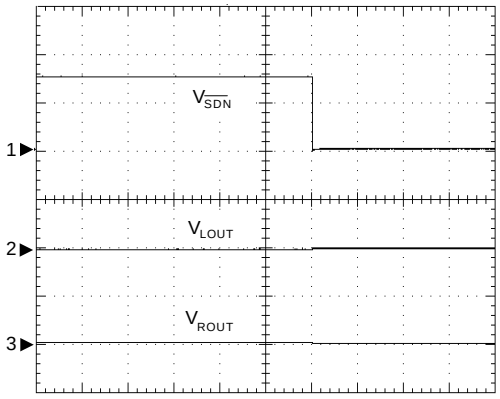
V_{DD}=3.6V, R_L=32Ω
CH1: $V_{\overline{RSD}}$, 2V/Div, DC
CH2: V_{ROUT}, 1V/Div, DC
TIME:2ms/Div

Output Transient at Shutdown Release



V_{DD}=3.6V, R_L=32Ω
CH1: $V_{\overline{SDN}}$, 2V/Div, DC
CH2: V_{LOUT}, 20mV/Div, DC
CH3: V_{ROUT}, 20mV/Div, DC
TIME:2ms/Div

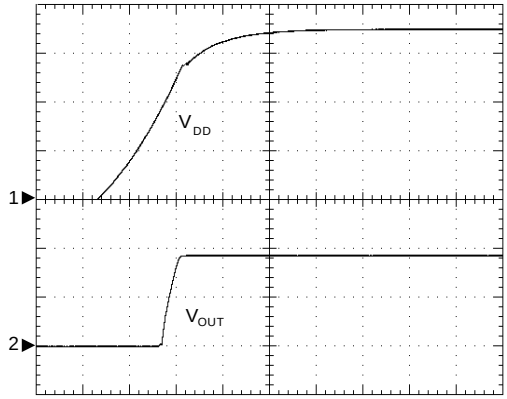
Output Transient at Shutdown



V_{DD}=3.6V, R_L=32Ω
CH1: $V_{\overline{SDN}}$, 2V/Div, DC
CH2: V_{LOUT}, 20mV/Div, DC
CH3: V_{ROUT}, 20mV/Div, DC
TIME:2ms/Div

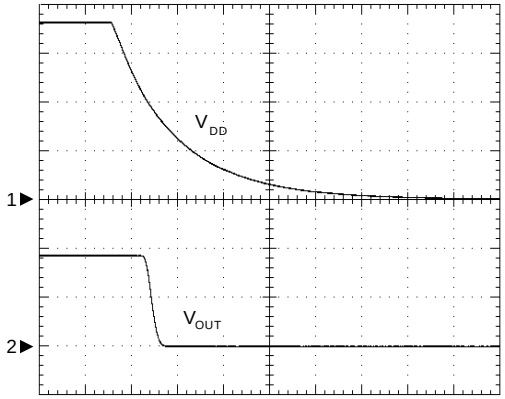
Operating Waveforms (Cont.)

VOUT Power On



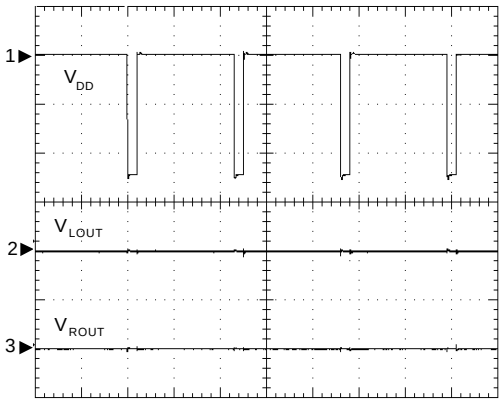
V_{DD}=3.6V, R_{OUT}=10kΩ
CH1: V_{DD}, 1V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
TIME:4ms/Div

VOUT Power Off



V_{DD}=3.6V, R_{OUT}=10kΩ
CH1: V_{DD}, 1V/Div, DC
CH2: V_{OUT}, 1V/Div, DC
TIME:10ms/Div

GSM Power Supply Rejection vs. Time

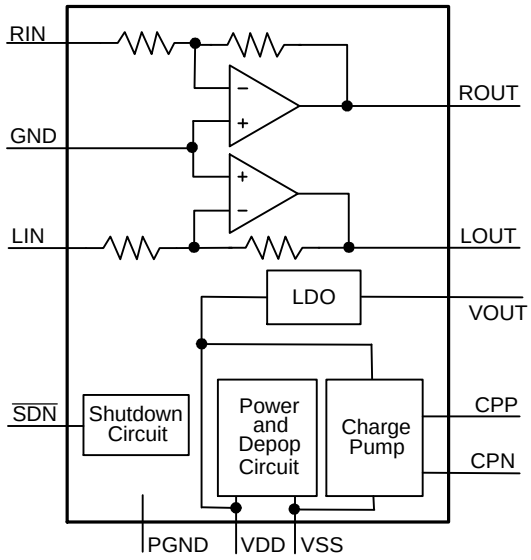


V_{DD}=3.6V, R_L=32Ω
CH1: V_{DD}, 200mV/Div, DC, Offset=3.6V
CH2: V_{LOUT}, 20mV/Div, DC
CH3: V_{ROUT}, 20mV/Div, DC
TIME:2ms/Div

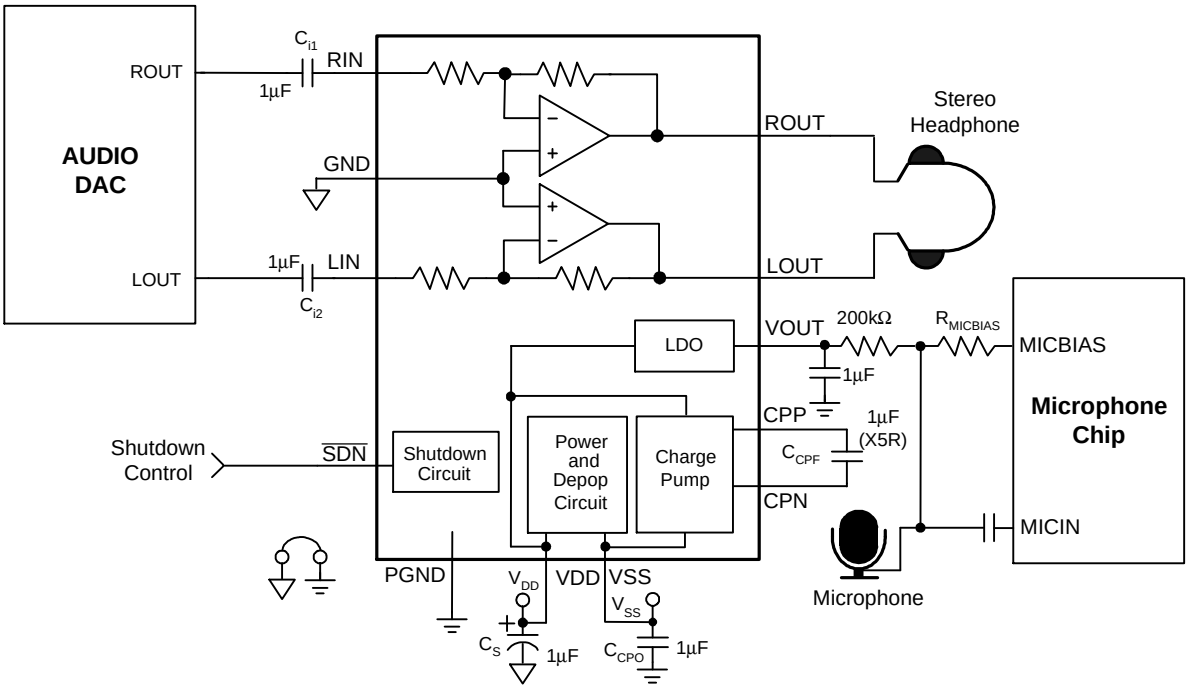
Pin Description

PIN		I/O/P	FUNCTION
NO.	NAME		
A1	VOUT	O	LDO (Low Drop-Out Regulator)'s output pin.
A2	CPN	I/O	Charge pump flying capacitor negative connection.
A3	PGND	P	Charge pump's ground.
A4	CPP	I/O	Charge pump flying capacitor positive connection.
B1	VSS	P	Headphone driver negative power supply.
B2	$\overline{SDN}$	I	Shutdown mod control input signal, pull low for shutdown headphone driver.
B3	GND	P	Ground connection for circuitry.
B4	VDD	P	Supply voltage input pin.
C1	LOUT	O	Left channel output for headphone.
C2	ROUT	O	Right channel output for headphone.
C3	LIN	I	Left channel input terminal.
C4	RIN	I	Right channel input terminal.

Block Diagram



Typical Application Circuit



Function Description

Headphone Driver Operation

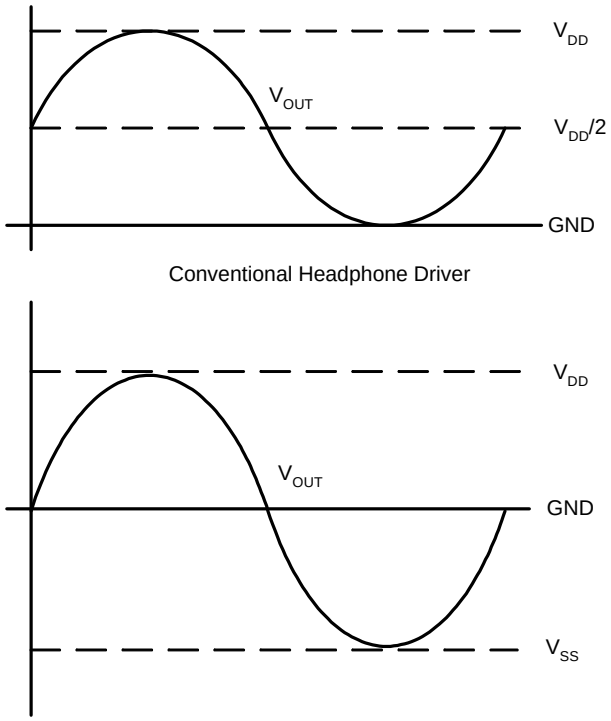


Figure 1. Cap-free Operation

The APA2181's headphone drivers use a charge pump to invert the positive power supply (V_{DD}) to negative power supply (V_{SS}), see figure1. The headphone drivers operate at this bipolar power supply (V_{DD} and V_{SS}) and the outputs reference refers to the ground. This feature eliminates the output capacitor that is using in conventional single-ended headphone drive amplifier. Compare with the single power supply amplifier, the power supply range has almost doubled.

Thermal Protection

The thermal protection circuit limits the junction temperature of the APA2181. When the junction temperature exceeds T_J = +150 °C, a thermal sensor turns off the driver, allowing the devices to cool. The thermal sensor allows the driver to start-up after the junction temperature down about 125°C. The thermal protection is designed with a 25°C hysteresis to lower the average T_J during continuous thermal overload conditions, increasing lifetime of the ICs.

Shutdown Function

In order to reduce power consumption while not in use, the APA2181 contains shutdown controllers to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when logic low is placed on the $\overline{SDN}$ pins for the APA2181. The trigger point between a logic high is 1.0V and logic low level is 0.35V. It is recommended to switch between ground and the supply voltage V_{DD} to provide maximum device performance. By switching the $\overline{SDN}$ pins to a low level, the amplifier enters a low-consumption current circumstance, charge pump is disabled, and I_{DD} for the APA2181 is in shutdown mode. In normal operating, the APA2181's $\overline{SDN}$ pins should be pulled to a high level to keep the IC out of the shutdown mode. The $\overline{SDN}$ pins should be tied to a definite voltage to avoid unwanted circumstance changes.

Low Drop-Out (LDO) Regulator

The LDO regulator's output provides maximum 5mA drive capacity for external audio codec. A 1µF decoupling capacitor with 0.1µF capacitor (filtering the high frequency noise) is recommended at LDO regulator's output. The LDO monitors the output current and limits the maximum output current to prevent damages during current overload or short circuit conditions.

The LDO provides a soft-start function, using the constant current to charge the output capacitor that gives a rapid and linear output voltage rise. If the load current is above the current limit start-up, the LDO cannot start successfully.

Application Information

Charge Pump Flying Capacitor (C_{CPF})

The flying capacitor (C_{CPF}) affects the load transient of the charge pump. If the capacitor's value is too small, and then this increases charge pump's output resistance and degrades the performance of headphone amplifier. Increasing the flying capacitor's value improves the load transient of charge pump. It is recommend to use the low ESR ceramic capacitors (X5R or X7R type is recommended) above 1µF.

Charge Pump Output Capacitor (C_{CPO})

The charge pump needs an output capacitor(C_{CPO}) to filter the negative output current pulse flowing into CVSS pin as well as reduces the output voltage ripple(CVSS). The capacitor also sucks in surge current flowing from the V_{SS} pin, the negative power input pin for the amplifiers. The output ripple is determined by the capacitance, ESR, and current ripple of the output capacitor. Increasing the value of output capacitor and decreasing the ESR can reduce the voltage ripple. Using a low-ESR ceramic capacitor greater than 1µF is recommended. For reducing the parasitic inductance and improving the noise decoupling, place the capacitor near the CVSS and PGND pins as close as possible.

Input Capacitor (C_i)

In the typical application, an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_i and the input impedance R_i from a high-pass filter with the cutoff frequency are determined in the following equation:

$$f_{C(highpass)} = \frac{1}{2\pi R_i C_i} \quad (1)$$

The value of C_i must be considered carefully because it directly affects the low frequency performance of the circuit. Consider the example where R_i is 14kΩ and the specification that calls for a flat bass response down to 10Hz. The equation is reconfigured as below:

$$C_i = \frac{1}{2\pi R_i f_C} \quad (2)$$

When input resistance variation is considered, the C_i is 1µF. Therefore, a value in the range of 1µF to 2.2µF would be chosen. A further consideration for this capacitor is the leakage path from the input source through the input network (R_i + R_f, C_i) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the negative side of the capacitor should face the amplifiers' inputs in most applications because the DC level of the amplifiers' inputs are held at 0V. Please note that it is important to confirm the capacitor polarity in the application.

Power Supply Decoupling (C_S)

The APA2181 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) as low as possible. Power supply decoupling also prevents the oscillations being caused by long lead length between the amplifier and the speaker.

The optimum decoupling is achieved by using two different types of capacitor that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series- resistance (ESR) ceramic capacitor, typically 0.1µF, is placed as close as possible to the device VDD lead for the best performance. For filtering lower frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Thermal Consideration

Linear power amplifiers dissipate a significant amount of heat in the package in normal operating condition. The first consideration to calculate maximum ambient tem peratures is the numbers from the Power Dissipation vs. Output Power graphs are per channel values, so the dissipation of the IC heat needs to be doubled for two-channel operation. Given θ_{JA}, the maximum allowable junction temperature (T_{JMax}), the total internal dissipation (P_D), and the maximum ambient temperature can be calcu-

Application Information (Cont.)

Thermal Consideration (Cont.)

lated with the following equation. The maximum recommended junction temperature for the APA2181 is 150°C. The internal dissipation figures are taken from the Power Dissipation vs. Output Power graphs. The APA2181 is designed with a thermal shutdown protection that turns the device off when the junction temperature surpasses 150° C to prevent damaging the IC.

Layout Consideration

1. All components should be placed close to the APA2181. For example, the input capacitor (C_{iR}, C_{iL}) should be close to APA2181 input pins to avoid causing noise coupling to APA2181 high impedance inputs; the decoupling capacitor (C_S) should be placed by the APA2181 power pin to decouple the power rail noise.
2. The output traces should be short, wide (>50mil), and symmetric.
3. The input trace should be short and symmetric.
4. The power trace width should be greater than 50mil.
5. The input trace and output trace should be away from C_{CPF} and C_{CPB} possible.

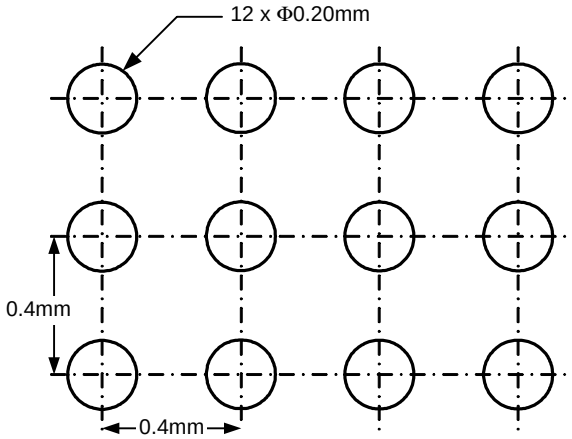


Figure 2. WLCSP2x2-16 land pattern recommendation

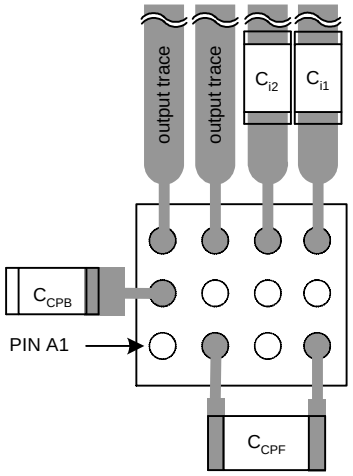
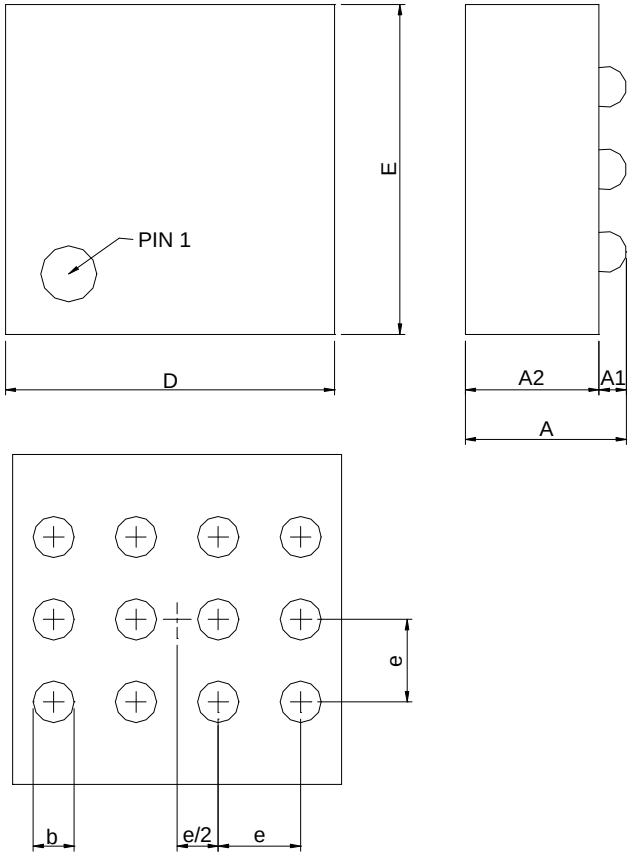


Figure 3. APA2181 Layout Suggestion

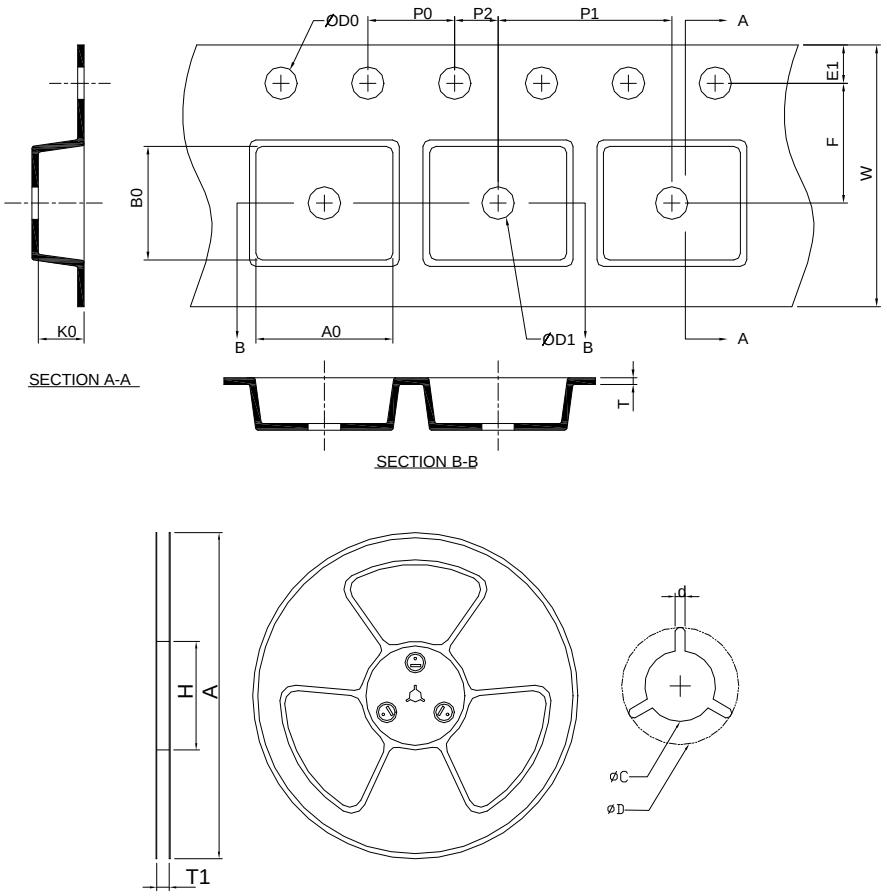
Package Information

WLCSP1.6x1.6-12



SYMBOL	WLCSP1.6x1.6-12			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.45	0.55	0.017	0.022
A1	0.10	0.20	0.004	0.008
A2	0.55	0.75	0.022	0.030
b	0.15	0.25	0.006	0.010
D	1.50	1.60	0.059	0.063
E	1.50	1.60	0.059	0.063
e	0.4 BSC		0.016 BSC	

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
WLCSP1.6x1.6-12	178.0±2.00	50 MIN.	8.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	8.0±0.30	1.75±0.10	3.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	4.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	1.75±0.15	1.75±0.15	0.75±0.10

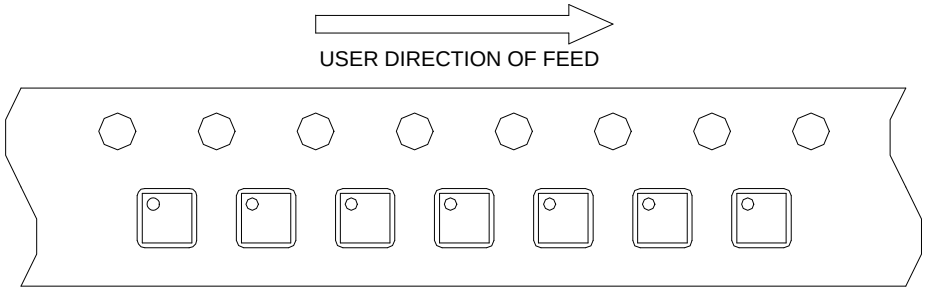
(mm)

Devices Per Unit

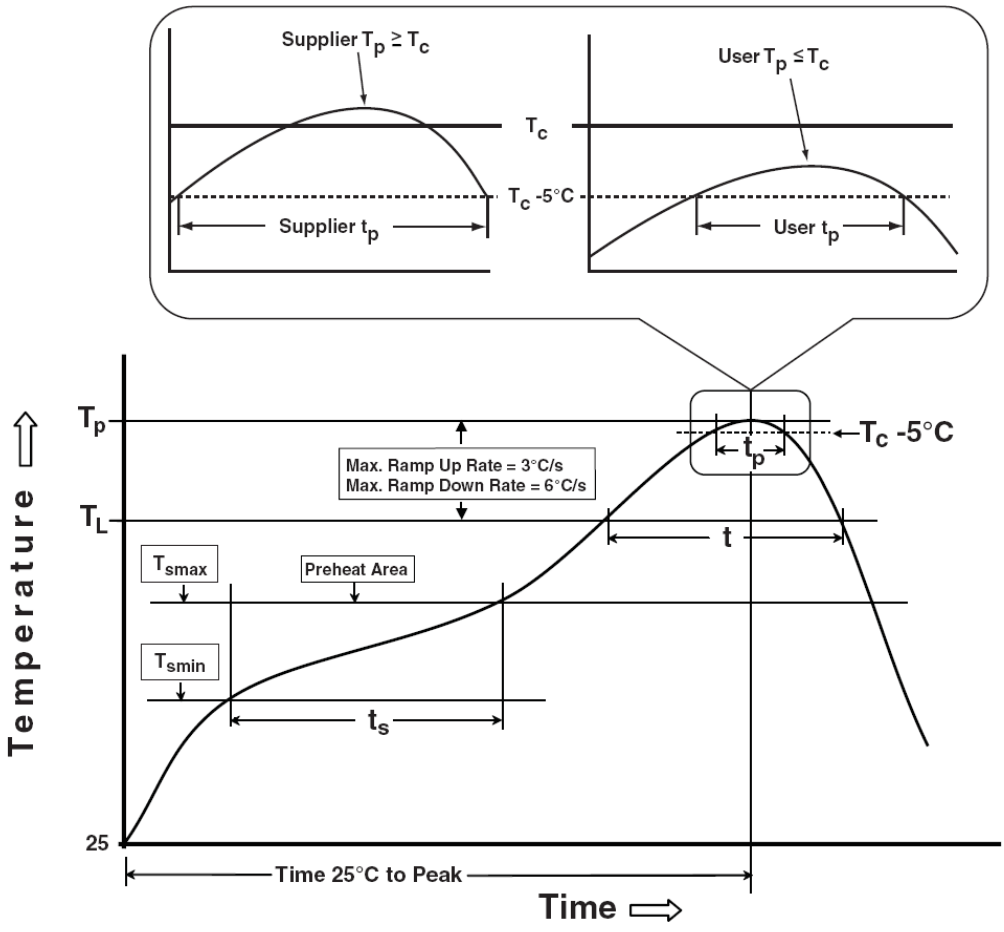
Package Type	Unit	Quantity
WLCSP1.6x1.6-12	Tape & Reel	3000

Taping Direction Information

WLCSP1.6x1.6-12



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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